

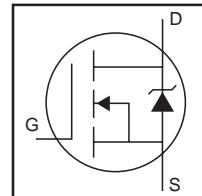
IRFB3307PbF
IRFS3307PbF
IRFSL3307PbF

Applications

- High Efficiency Synchronous Rectification in SMPS
- Uninterruptible Power Supply
- High Speed Power Switching
- Hard Switched and High Frequency Circuits

Benefits

- Improved Gate, Avalanche and Dynamic dV/dt Ruggedness
- Fully Characterized Capacitance and Avalanche SOA
- Enhanced body diode dV/dt and dI/dt Capability
- Lead-Free



V_{DSS}	75V
R_{DS(on)} typ.	5.0mΩ
max.	6.3mΩ

HEXFET® Power MOSFET



Absolute Maximum Ratings

Symbol	Parameter	Max.	Units
I _D @ T _C = 25°C	Continuous Drain Current, V _{GS} @ 10V	120①②	A
I _D @ T _C = 100°C	Continuous Drain Current, V _{GS} @ 10V	84①②	
I _{DM}	Pulsed Drain Current ②	510	
P _D @ T _C = 25°C	Maximum Power Dissipation	200①	W
	Linear Derating Factor	1.3①	W/°C
V _{GS}	Gate-to-Source Voltage	± 20	V
dV/dt	Peak Diode Recovery ④	11	V/ns
T _J	Operating Junction and	-55 to + 175	°C
T _{STG}	Storage Temperature Range		
	Soldering Temperature, for 10 seconds (1.6mm from case)		
	Mounting torque, 6-32 or M3 screw	300	
		10lb·in (1.1N·m)	

Avalanche Characteristics

E _{AS} (Thermally limited)	Single Pulse Avalanche Energy ③	270	mJ
I _{AR}	Avalanche Current ①	See Fig. 14, 15, 16a, 16b	A
E _{AR}	Repetitive Avalanche Energy ⑤		

Thermal Resistance

Symbol	Parameter	Typ.	Max.	Units
R _{θJC}	Junction-to-Case ⑨	—	0.61①	°C/W
R _{θCS}	Case-to-Sink, Flat Greased Surface , TO-220	0.50	—	
R _{θJA}	Junction-to-Ambient, TO-220 ⑨	—	62	
R _{θJA}	Junction-to-Ambient (PCB Mount) , D ² Pak ⑧⑨	—	40	

Static @ $T_J = 25^\circ\text{C}$ (unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(\text{BR})\text{DSS}}$	Drain-to-Source Breakdown Voltage	75	—	—	V	$V_{GS} = 0\text{V}$, $I_D = 250\mu\text{A}$
$\Delta V_{(\text{BR})\text{DSS}}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	—	0.069	—	V/ $^\circ\text{C}$	Reference to 25°C , $I_D = 1\text{mA}$ ②
$R_{DS(\text{on})}$	Static Drain-to-Source On-Resistance	—	5.0	6.3	$\text{m}\Omega$	$V_{GS} = 10\text{V}$, $I_D = 75\text{A}$ ⑤
$V_{GS(\text{th})}$	Gate Threshold Voltage	2.0	—	4.0	V	$V_{DS} = V_{GS}$, $I_D = 150\mu\text{A}$
	Drain-to-Source Leakage Current	—	—	20	μA	$V_{DS} = 75\text{V}$, $V_{GS} = 0\text{V}$
I_{GSS}	—	—	250	—		$V_{DS} = 75\text{V}$, $V_{GS} = 0\text{V}$, $T_J = 125^\circ\text{C}$
	Gate-to-Source Forward Leakage	—	—	200	nA	$V_{GS} = 20\text{V}$
I_{GRR}	Gate-to-Source Reverse Leakage	—	—	-200		$V_{GS} = -20\text{V}$
R_G	Gate Input Resistance	—	1.5	—	Ω	f = 1MHz, open drain

Dynamic @ $T_J = 25^\circ\text{C}$ (unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
g_{fs}	Forward Transconductance	98	—	—	S	$V_{DS} = 50\text{V}$, $I_D = 75\text{A}$
Q_g	Total Gate Charge	—	120	180	nC	$I_D = 75\text{A}$
Q_{gs}	Gate-to-Source Charge	—	35	—		$V_{DS} = 60\text{V}$
Q_{gd}	Gate-to-Drain ("Miller") Charge	—	46	—		$V_{GS} = 10\text{V}$ ⑤
$t_{d(on)}$	Turn-On Delay Time	—	26	—	ns	$V_{DD} = 48\text{V}$
t_r	Rise Time	—	120	—		$I_D = 75\text{A}$
$t_{d(off)}$	Turn-Off Delay Time	—	51	—		$R_G = 3.9\Omega$
t_f	Fall Time	—	63	—		$V_{GS} = 10\text{V}$ ⑤
C_{iss}	Input Capacitance	—	5150	—	pF	$V_{GS} = 0\text{V}$
C_{oss}	Output Capacitance	—	460	—		$V_{DS} = 50\text{V}$
C_{rss}	Reverse Transfer Capacitance	—	250	—		$f = 1.0\text{MHz}$
C_{oss} eff. (ER)	Effective Output Capacitance (Energy Related)	—	570	—		$V_{GS} = 0\text{V}$, $V_{DS} = 0\text{V}$ to 60V ⑦, See Fig.11
C_{oss} eff. (TR)	Effective Output Capacitance (Time Related) ⑥	—	700	—		$V_{GS} = 0\text{V}$, $V_{DS} = 0\text{V}$ to 60V ⑥, See Fig. 5

Diode Characteristics

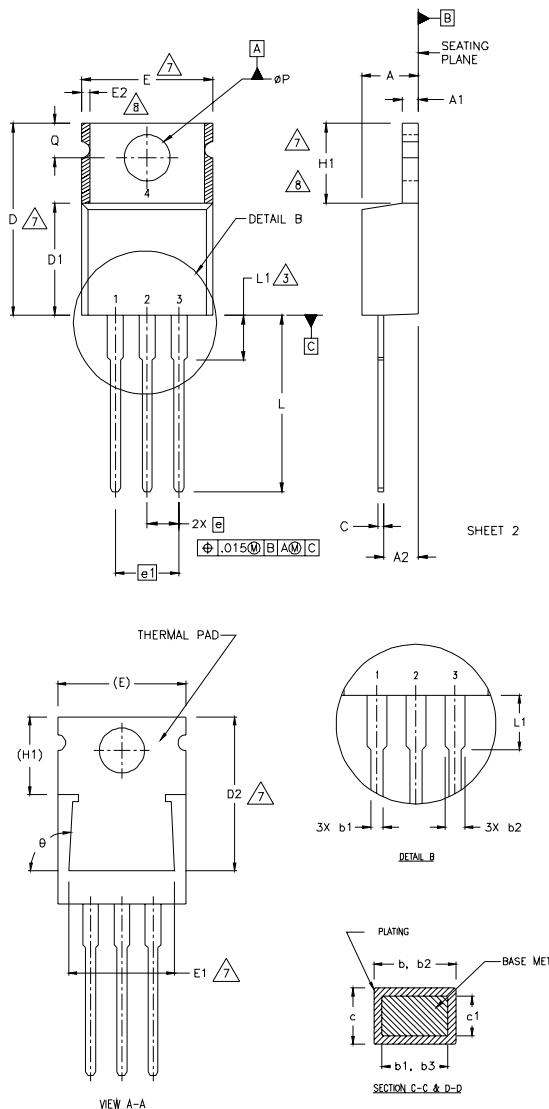
Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
I_s	Continuous Source Current (Body Diode)	—	—	120①	A	MOSFET symbol showing the integral reverse p-n junction diode.
I_{SM}	Pulsed Source Current (Body Diode) ②	—	—	510	A	
V_{SD}	Diode Forward Voltage	—	—	1.3	V	$T_J = 25^\circ\text{C}$, $I_s = 75\text{A}$, $V_{GS} = 0\text{V}$ ⑤
t_{rr}	Reverse Recovery Time	—	38	57	ns	$T_J = 25^\circ\text{C}$ $V_R = 64\text{V}$,
		—	46	69		$T_J = 125^\circ\text{C}$ $I_F = 75\text{A}$
Q_{rr}	Reverse Recovery Charge	—	65	98	nC	$T_J = 25^\circ\text{C}$ $\frac{di}{dt} = 100\text{A}/\mu\text{s}$ ⑤
		—	86	130		$T_J = 125^\circ\text{C}$
I_{IRR}	Reverse Recovery Current	—	2.8	—	A	$T_J = 25^\circ\text{C}$
t_{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by LS+LD)				

Notes:

- ① Calculated continuous current based on maximum allowable junction temperature. Package limitation current is 75A.
- ② Repetitive rating; pulse width limited by max. junction temperature.
- ③ Limited by $T_{J\text{max}}$, starting $T_J = 25^\circ\text{C}$, $L = 0.096\text{mH}$
 $R_G = 25\Omega$, $I_{AS} = 75\text{A}$, $V_{GS} = 10\text{V}$. Part not recommended for use above this value.
- ④ $I_{SD} \leq 75\text{A}$, $\frac{di}{dt} \leq 530\text{A}/\mu\text{s}$, $V_{DD} \leq V_{(\text{BR})\text{DSS}}$, $T_J \leq 175^\circ\text{C}$.
- ⑤ Pulse width $\leq 400\mu\text{s}$; duty cycle $\leq 2\%$.
- ⑥ C_{oss} eff. (TR) is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 to 80% V_{DSS} .
- ⑦ C_{oss} eff. (ER) is a fixed capacitance that gives the same energy as C_{oss} while V_{DS} is rising from 0 to 80% V_{DSS} .
- ⑧ When mounted on 1" square PCB (FR-4 or G-10 Material). For recommended footprint and soldering techniques refer to application note #AN-994.
- ⑨ R_θ is measured at T_J approximately 90°C .
- ⑩ $R_{\theta,JC}$ (end of life) for D²Pak and TO-262 = $0.75^\circ\text{C}/\text{W}$. Note: This is the maximum measured value after 1000 temperature cycles from -55 to 150°C and is accounted for by the physical wearout of the die attach medium.

TO-220AB Package Outline

Dimensions are shown in millimeters (inches)



NOTES:

- 1 DIMENSIONING AND TOLERANCING PER ASME Y14.5 M- 1994.
- 2 DIMENSIONS ARE SHOWN IN INCHES [MILLIMETERS].
- 3 LEAD DIMENSION AND FINISH UNCONTROLLED IN L1.
- 4 DIMENSION D & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED .005" (.127) PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY.
- 5 CONTROLLING DIMENSION : INCHES.
- 6 THERMAL PAD CONTOUR OPTIONAL WITHIN DIMENSIONS E,H1,D2 & E1
- 7 DIMENSION E2 X H1 DEFINE A ZONE WHERE STAMPING AND SINGULATION IRREGULARITIES ARE ALLOWED.

LEAD ASSIGNMENTSHOTFET

- 1.- GATE
2.- DRAIN
3.- SOURCE

IGBTs, CoPACK

- 1.- GATE
2.- COLLECTOR
3.- Emitter

DIODES

- 1.- ANODE/OPEN
2.- CATHODE
3.- ANODE

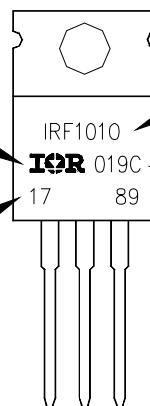
SYMBOL	DIMENSIONS				NOTES	
	MILLIMETERS		INCHES			
	MIN.	MAX.	MIN.	MAX.		
A	3.56	4.82	.140	.190		
A1	0.51	1.40	.020	.055		
A2	2.04	2.92	.080	.115		
b	0.38	1.01	.015	.040		
b1	0.38	0.96	.015	.038	5	
b2	1.15	1.77	.045	.070		
b3	1.15	1.73	.045	.068		
c	0.36	0.61	.014	.024		
c1	0.36	0.56	.014	.022	5	
D	14.22	16.51	.560	.650		
D1	8.38	9.02	.330	.355		
D2	12.19	12.88	.480	.507	7	
E	9.66	10.66	.380	.420	4,7	
E1	8.38	8.89	.330	.350	7	
e	2.54 BSC		.100 BSC			
e1	5.08		.200 BSC			
H1	5.85	6.55	.230	.270		
L	12.70	14.73	.500	.580		
L1	-	6.35	-	.250		
ØP	3.54	4.08	.139	.161		
Q	2.54	3.42	.100	.135		
Ø	90°-93°		90°-93°			

TO-220AB Part Marking Information

EXAMPLE: THIS IS AN IRF1010
LOT CODE 1789
ASSEMBLED ON WW 19, 2000
IN THE ASSEMBLY LINE "C"

Note: "P" in assembly line position indicates "Lead - Free"

INTERNATIONAL
RECTIFIER
LOGO
ASSEMBLY
LOT CODE



PART NUMBER
DATE CODE
YEAR 0 = 2000
WEEK 19
LINE C

TO-220AB packages are not recommended for Surface Mount Application.